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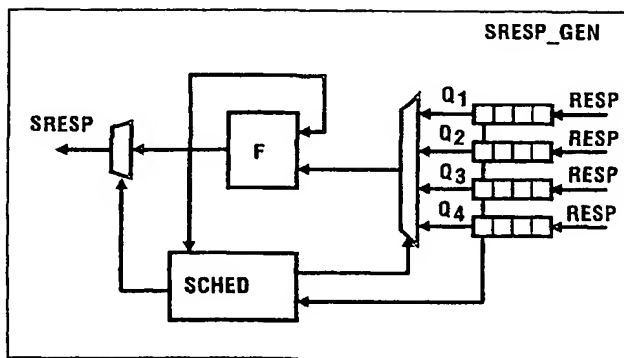
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[Continued on next page]

(54) Title: INTEGRATED CIRCUIT AND METHOD FOR ESTABLISHING TRANSACTIONS

NI



(57) Abstract: An integrated circuit (IC) comprises a network and a plurality of modules (M1, M2, M3) which communicate to each other via the network. A first module (M1) sends a plurality of requests (REQ) to at least two second modules (M2, M3, Mn) and the second modules send individual responses (RESP2, RESP3, RESPn) to the first module, indicating a result of the execution of the requests. The integrated circuit (IC) comprises a network capable of sending a single response (SRESP) to the first module (M1) dependent on the individual responses (RESP2, RESP3 up to and including RESPn) from the second modules (M2, M3, Mn). The single response (SRESP) can indicate that at least one second module has executed the requests (REQ) or that a specific error has occurred in at least one of the second modules (M2, M3, Mn). The single response (SRESP) can also indicate which types of error have occurred in the second modules (M2, M3, Mn). If various errors have occurred, the single response (SRESP) can indicate which error is the most serious error or information about all errors.

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DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

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# INTERNATIONAL SEARCH REPORT

International Application No  
PCT/IB 03/04401

A. CLASSIFICATION OF SUBJECT MATTER  
IPC 7 H04L12/56 H04L29/06 H04L12/28

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)  
IPC 7 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	DATABASE 'Online! S KUMAR ET AL: "A Network on Chip Architecture and Design Methodology" retrieved from CSDL.COMPUTER.ORG/COMP/PROCEEDINGS/ISVLSI/ 2002/1486/00/14860117ABS.HTM XP002263346 page 1, right-hand column, line 11 -page 2, right-hand column, line 14 page 3, left-hand column, line 13 -page 6, left-hand column, line 27; figures 1-4 ---	1-9
Y	WO 02 23814 A (SUN MICROSYSTEMS INC) 21 March 2002 (2002-03-21) page 3, line 12 -page 4, line 23 page 5, line 8 - line 30; claims 1-25; figures 3-6,8,9 --- -/--	1-9

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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International Application No  
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	GUERRIER P ET AL: "A Generic Architecture for On-Chip Packet-Switched Interconnections" 27 March 2000 (2000-03-27), pages 250-256, XP010377472	1-3,8,9
A	page 251, left-hand column, line 10 -page 253, right-hand column, line 17 page 254, right-hand column, line 1 - line 54; figures 2-8	4-7
Y	MOON SANG-JUN ET AL: "Scalable and reliable ATM multicast employing RM cell consolidation" ELECTRONICS LETTERS, IEE STEVENAGE, GB, vol. 35, no. 23, 11 November 1999 (1999-11-11), pages 2008-2009, XP006012937 ISSN: 0013-5194	1-3,8,9
A	page 1, left-hand column, line 1 -right-hand column, line 38	4-7

Inter            nal Application No

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Publication date

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